IT IS CLAIMED:

1. A memory system circuit, comprising:

a controller; and

a memory comprising a plurality of independently controllable non-volatile data storage sections connected to the controller so that data is transferable from the controller to a second of the data storage sections while data is being programmed into a first data storage of the data storage sections.

2. The memory system circuit of claim 1, further comprising:

a bus connected to transfer data between the controller and the data storage sections whereby data is transferable to the second data storage section while data is being programmed into the first data storage section.

3. The memory system circuit of claim 2, wherein the controller comprises a first and a second data buffer wherein data is stored for transfer to the first and second data storage sections.

4. The memory system circuit of claim 2, wherein each of the data storage sections comprises a data register wherein data transferred from the controller is stored.

5. The memory system circuit of claim 4, wherein each of the data storage sections further comprises an array of non-volatile storage units into which data stored in the data register is programmed.

6. The memory system circuit of claim 4, wherein each of the data storage sections further comprises a RAM memory section connected to store a copy of the data transferred into the data register.

7. The memory system circuit of claim 1, wherein the controller, the first data storage section and the second data storage section are on separate chips.

8. The memory system circuit of claim 1, wherein the first data storage section and the second data storage section are on a single chip.

9. The memory system circuit of claim 1, wherein the controller, the first data storage section and the second data storage section are on a single chip.

10. The memory system circuit of claim 1, wherein the controller, the first data storage section and the second data storage section are part of a single card structure removably attachable to a host.

11. The memory system circuit of claim 1, wherein the controller is embedded in a host and wherein the first data storage section and the second data storage section are part of a single card structure removably attachable to the host.

12. A method of operating a non-volatile memory comprising a memory control circuit and a plurality of storage sections capable of independent operations initiated via an external interface, the method comprising:

transferring a first set of data from an external source to a first storage section; and

subsequent to said transferring the first set of data:

programming the first set of data into the first storage section; and

transferring a second set of data from the controller to a second storage section, wherein the transferring a second set of data occurs during the programming the first set of data.

13. The method of claim 12, further comprising:

subsequent to the transferring the second set of data, programming the second set of data into the second storage section, wherein programming the second set of data starts during the programming the first set of data.

14. The method of claim 13, further comprising:

subsequent to the programming the first set of data, performing an erase operation in the first storage section, wherein the erase operation starts during the programming the second set of data.

15. The method of claim 12, further comprising:

loading the first data set into a first register prior to programming the first set of data; and

loading a third set of data into the first register subsequent to the start of programming the first set of data and prior to completing the programming the first set of data.

16. The method of claim 15, wherein the transferring the first set of data from the external source to the first storage section comprises:

temporarily storing a first copy of the first data set in a first register in the first storage section; and

temporarily storing a second copy of the first data set in a second register in the first storage section; and

wherein the programming the first set of data into the first storage section comprises:

programming the first copy of the first data set from the first register into a non-volatile memory array in the first storage section.

17. The method of claim 16, wherein the programming the first set of data into the first storage section further comprises:

verifying the result of said writing the first copy of the first data set using the second copy the first data set.

18. The method of claim 12, wherein the first set of data comprises multiple sectors and wherein the programming the first set of data comprises programming multiple pages in the first storage section in parallel.

19. A method of operating a non-volatile memory comprising a memory control circuit and a plurality of storage sections capable of independent operations initiated via an external interface, the method comprising:

causing a first of the storage sections to be selected;

transferring a first set of data from an external source to the selected storage section through the external interface;

subsequent to the transferring a first set of data, causing the first of the storage sections to be deselected and a second of the storage sections to be selected;

subsequent to causing the second of the storage sections to be selected, transferring a second set of data from the external source selected storage section through the external interface; and

programming the first set of data, wherein the transferring the second set of data occurs during the programming the first set of data.

20. The method of claim 19, further comprising:

programming the second set of data, wherein programming the second set of data starts during the programming the first set of data.

21. The method of claim 20, further comprising:

subsequent to the programming the first set of data, performing an erase operation in the first storage section, wherein the erase operation starts during the programming the second set of data.

22. The method of claim 19, wherein the memory circuit comprises a first register, the method further comprising:

loading the first data set into the first register prior to programming the first set of data; and

loading a third set of data into the first register subsequent to the programming the first set of data and prior to completing the programming the first set of data.

23. The method of claim 22, wherein the first storage section comprises a register and a non-volatile memory array, and wherein the transferring the first set of data from an external source to the selected storage section comprises:

temporarily storing a first copy of the first set of data in a first register in the selected storage section; and

temporarily storing a second copy of the first set of data in a second register in the selected storage section; and

wherein the programming the first set of data comprises:

programming the first copy the first set of data from the register into the non-volatile memory array.

24. The method of claim 23, wherein the programming the first set of data further comprises:

verifying the result of said writing the first copy of the first set of data using the second copy of the first set of data.

25. The method of claim 19, wherein the first set of data comprises multiple sectors and wherein the programming the first set of data comprises programming multiple pages in the selected section in parallel.

26. A method of operating a non-volatile memory system, comprising a system controller and two or more independent non-volatile memory arrays, the method comprising:

receiving data in the controller via a host system interface;

transferring the data to a plurality of said non-volatile memory arrays in a pipelined manner; and

programming the transferred data into the non-volatile memory arrays, wherein the transferring of data to a first of the memory arrays occurs during the programming of transferred data in a second of the memory arrays.

27. The method of claims 26, wherein the program operation comprises programming multiple pages of data in parallel.

28. The method of claims 26, further comprising:

performing an erase operation in the non-volatile memory chips, wherein the performing an erase operation in the second of the memory arrays occurs subsequent to the programming of transferred data in the second of the memory arrays during the programming of transferred data in the first of the memory arrays.